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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,260	07/30/2003	Erin Antony Handgen	200205911-1	8717

22879 7590 05/17/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
DANG, KHANH	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,260	HANDGEN ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 2 and line 6, the word "logic" should be changed to – logic block -- . Further, the phrase "to interface" (line 2 and line 6, is unclear. As described in the originally filed specification, the logic block is a part or a component of the companion IC. See also claim 6. In line 5, after "and" -- . – must be deleted. In addition, claims 1-8 are directed to an apparatus. However, the essential structural cooperative relationships between the "first companion integrated circuit," "second companion integrated circuit," "first portion," "second portion," unified bus logic," and "functional logic" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

In claim 2, "logic" should be changed to – logic block – or –logic circuit --.

In claim 3, "functional logic" should be changed to – functional logic block – or functional logic circuit --.

In claim 6-8, claims 6-8 are directed to an apparatus. However, the essential structural cooperative relationships between the "host," "first," second," "third," and "additional" IC components have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01. Further, it is unclear

what may be the "third integrated circuit." Applicants are invited to point out to the specification the disclosure of the "third integrated circuit" as claimed.

In claim 7, it is unclear what may be the "at least one additional integrated circuit." Applicants are invited to point out to the specification the disclosure of the "at least one integrated circuit" as claimed.

In claim 8, "functional logic" should be changed to – functional logic block – or functional logic circuit --.

In claim 9, it is unclear what may be the structural relationships between the "integrated circuit component" and the "intermediate integrated circuit, ""second intermediate integrated circuit," "host integrated circuit." See MPEP 2172.01.

In claim 10, "logic" should be changed to – logic block – or –logic circuit --.

In claim 11, it is unclear what may be the structural relationships between the "integrated circuit component" and "logic portion," "companion integrated circuit, ""second intermediate integrated circuit," "host integrated circuit." See MPEP 2172.01.

In claim 12, "logic" should be changed to – logic block – or –logic circuit --.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al. (Estakhri, 6,172,906).

As broadly drafted, these claims do not define any structure that differs from Estakhri.

With regard to claim 1, Estakhri discloses an integrated circuit component (shown generally at Figs. 1 and 6a) comprising: logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic") capable of being configured to interface with a first companion integrated circuit (18/ or 670) and to receive information that is communicated from the first companion integrated circuit (18 or 670), which information was communicated to the first companion integrated circuit (18 or 670) via a first portion of a system bus (28/680); and. logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic") capable of being configured to interface with a second companion integrated circuit (20/672) and to receive information that is communicated from the second companion integrated circuit (20/672), which information was communicated to

the second companion integrated circuit (20/672) via a second portion of the system bus (38/684).

With regard to claim 2, it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both logic portions.

With regard to claim 3, it is clear that integrated circuit component further comprising functional logic (flash memory logic) for performing at least one logic operation (memory operation) for the integrated circuit component.

With regard to claim 4, it is clear that the system bus (680/684) is a point-to-point serial communication bus.

With regard to claim 5, it is clear that the first portion of the system bus is substantially one-half of the system bus and the second portion of the system bus is a remainder of the system bus (see at least column 7, lines 4-9).

With regard to claim 6, Estakhri discloses a system in which a plurality of companion integrated circuit components collectively implement a logic function embodied in a single, conventional integrated circuit component (shown generally at Fig. 1, 6(a, b) comprising: a host integrated circuit component (12/610/504) communicating with other integrated circuit components (16/506, for example) via a system bus (675); a first integrated circuit component (18/670) comprising logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic") for interfacing with a first portion (28/680) of system bus (275); a second integrated circuit component (20/672) comprising logic (since 506 is an digital IC

and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic") for interfacing with a second portion (38/684) of system bus (275); a third integrated circuit component (defined by flash storage 669 and 674) not directly coupled with the system bus (675) and comprising logic (it is clear flash memory operations must comprise "logic") for communicating with the host integrated circuit (14/610) via the first and second integrated circuit components (18/670 or 20/672).

With regard to claim 8, it is clear that the third integrated circuit further comprising functional logic (memory operation logic, for example) that performs a conventional functional operation (memory operation).

With regard to claim 9, Estakhri discloses an integrated circuit component comprising: a first set of conductive pins (it is clearly inherent that flash memory 669/674 must comprise pins for providing electrical connections and communication) for channeling communications to a host integrated circuit (14/610/504) through a first intermediate integrated circuit (18/670), the first intermediate integrated circuit (18/670) being in direct communication with the host integrated circuit via a first portion (28/680) of a system bus (275) ; and a second set of conductive pins for channeling communications to the host integrated circuit (14/610/504) through a second intermediate integrated circuit (20/672), the second intermediate integrated circuit (20/672) being in direct communication with the host integrated circuit (14/610/504) via a second portion (38/684) of the system bus.

With regard to claim 10, it is clear that the integrated circuit component further comprises unified bus logic (provided by controller 12/510) configured to consolidate information received from the channeled communications through the first and second set of conductive pins.

With regard to claim 11, at the outset, it is noted that the word "or" indicates that only one condition is needed for the prior art to meet the claim limitations. In any event, Estakhri discloses an integrated circuit component comprising two independent logic portions (provided by chips 18/670 or 20/672), each logic portion being capable of being alternatively configured to either communicate with a host integrated circuit (14/610/504) via a portion (28/680 or 38/684) of a system bus or communicate with a companion integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit (the other of 18/670 or 20/672), which information was communicated to the companion integrated circuit via a portion (28/680 or 38/684) of a system bus.

With regard to claim 12, the integrated circuit component further comprises unified bus logic (provided by controller 12/510) configured to consolidate information received from both logic portions.

Non-Statutory Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent

and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-12 are provisionally rejected under the judicially created doctrine of the obviousness-type double patenting of claims 1-12, 15-24 of copending Application No. 10/630,460. Although the conflicting claims are not identical, they are not patentably distinct from each other because the difference in wordings between the claims clearly does not constitute any patentable distinction. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

It is well settled that it is unobviousness in the overall appearance of the claimed design, when compared with the prior art, rather than minute details or small variations in design as appears to be the case here, that constitutes the test of design

patentability. See *In re Frick*, 275 F2d 741, 125 USPQ 191 (CCPA 1960) and *In re Lamb,* 286 F2d 610, 128 USPQ 539 (CCPA 1961).

US. Patent Nos. 6,182,178 TO Kelley, 5,862,359 to Nozuyama, and US 2005/0014397 to Brown are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Examiner